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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,920	02/02/2001	James J. Alwan	100.718.419 (MIC- 77US)	8909

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EXAMINER	
MACCHIAROLO, PETER J	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,920	ALWAN, JAMES J.	
	Examiner	Art Unit	
	Peter J. Macchiarolo	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-26 and 33-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-26 and 33-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The reply filed on 08/31/2006 consists of changes to the specification, drawings, and to the claims, and further, the reply consists of remarks related to the prior rejection of claims in the previous Office Action. The above have been entered and considered. However, pending claims 13-26, and 33-45 are not allowable as explained below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-26, and 33-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of previously cited Fishkin et al (USPN 6202658; "Fishkin") in further view of previously cited Potter (USPN 5700176; "Potter").

Regarding claims 13-21, 24, and 39, AAPA discloses a method of forming an FED comprising providing a substrate having a central area and a peripheral area, forming alignment marks and bond pads on the peripheral area of the substrate, forming an emitter electrode structure on the central area of the substrate, forming a plurality of micropoints in groups on the emitter electrode structure, depositing an insulating layer over the substrate, emitter electrode structure, and plurality of micropoints, and depositing a conductive layer over the insulating layer. Applicant further admits it is known that selectively etching openings through the

conductive and insulating layers comprises applying a layer of photoresist on said conductive layer, imaging said photoresist to define a pattern for said openings, developing the photoresist, and etching the pattern for the openings (see for example instant specification, page 3 paragraph 3). The Examiner further notes that the prosecution history has also shown this to be a well-known method of manufacture.

Applicant further admits a method of making a semiconductor wafer to clear alignment marks by locally applying a wet etchant to uncover a structure is known in the art to effectively clear the marks without the use of photolithography (instant specification page 4, paragraph 2). Fishkin also supports this teaching in column 2 line 47 to column 3 line 10, that using a wet etchant to clean the edge of a wafer allows for a wafer cleaner which requires minimal additional parts and manufacturing time, and further teaches this method requires moving an etchant dispenser or the cathode assembly relative to one another during the applying while selectively spraying a wet etchant on a structure (see at least the abstract).

Fishkin and AAPA are silent to using this method to manufacture an FED, or to the exact distance away from the alignment mark structure the etchant is applied.

However, Potter teaches in the abstract and in at least column 1 lines 23-32 that processes used to manufacture FED's utilize processes and equipment similar to those used for semiconductor fabrication, which allows a wide range of materials with less stringent controls of material purity. Further, Potter shows in figure 1, a cathode (100) and an anode (70) assembly assembled together in a FED, which can be automatically aligned, or aligned according to the well-known prior art method i.e. with alignment marks. Potter further teaches contact pads are

selectively provided at the device top surface to make electrical contact, which may require the same clearing method as described in Fishkin.

Furthermore, Fishkin and AAPA both infer applying etchant within 200 microns of the structure since Fishkin and AAPA disclose the etchant is used to uncover and clean the edge of a wafer. One of ordinary skill in the art will immediately recognize in order to uncover the structure with a wet etchant, the etchant must be applied directly on top of the structure to effectively uncover it, the distance then being approximately zero microns, thereby falling into the claimed range of 200 microns.

Even if, arguendo, Fishkin, Potter, or AAPA did not infer this exact distance, this is a matter of obvious design choice, since Applicant has not adequately disclosed any testing or analytical data which establishes criticality for these modifications, or recites any specific advantage the invention benefits from over the prior art from this modification. Further, one would arrive at this distance for a variety of reasons, such as to effectively clear the structure while reducing the time and cost of the manufacturing processes.

Therefore, in view of the above discussion, it would have been obvious to one having ordinary skill in the art at the time the invention was made to construct an FED with the method of AAPA and Fishkin with the etchant being applied within 200 microns of the structure to allow for less pure materials and cheaper manufacturing method.

Regarding claims 22, and 23, Applicant admits the prior art includes a method of forming a cathode assembly of a field emission device comprising polishing the conductive layer via

chemical-mechanical planarization. The Examiner further notes that the prosecution history has shown this to be a well known method of manufacture.

Regarding claim 25, most of the limitations herein have been previously discussed above, with the exception of forming a plurality of micropoints on the emitter electrode structure, depositing an insulating layer over the substrate, emitter electrode structure, and a plurality of micropoints; with walls defining the openings being spaced away from the micropoints. Not only does Potter teach this configuration, this is a well-known configuration of an FED. The reasons for combining and motivation are the same as for rejected claim 13 above.

Regarding claim 26, 33, 34, 37, 38, and 42-45 the limitations herein have been discussed at rejected claims 13 and 16 above and will not be repeated here. The reasons for combining and motivation are the same as for claim 13.

Regarding claim 35, 40, Fishkin shows in figure 5 applying the etchant on the periphery in elongated spray zones.

Regarding claims 36, and 41, Fishkin shows applying an etchant from a nozzle in the etchant dispenser while moving the nozzle over the device, but is silent to moving the nozzle linearly.

However, this is an obvious modification if the bond pads are in a linear configuration, as in an FED of Potter. The motivation and reasons for combining are the same as for claim 13.

Response to Arguments

Applicant's arguments filed 08/31/2006 have been fully considered but they are not persuasive.

First, Applicant alleges that neither Fishkin nor Yamasaki teach or suggest applying the wet etchant within 200 microns of the structure. However, as discussed above, both AAPA and Fishkin infers the distance is zero microns, since the wet etchant is corrosive and must be contiguous with the unwanted structure to properly etch it away. Furthermore, one of ordinary skill in the art will find this an obvious method, since the etchant is required to physically touch the structure to etch it. Therefore, the wet etchant should be applied within 200 microns of the structure to etch it properly.

Second, Applicant alleges, "Fishkin cannot infer this limitation as it fails to teach or suggest applying an etchant locally to uncover a structure in the peripheral area of the cathode assembly." Firstly, this argument is unclear. It appears Applicant is arguing Fishkin does not teach or suggest the etchant is locally applied to a peripheral area of a cathode to etch a structure. To this, the Examiner respectfully disagrees and reiterates that Fishkin was relied upon to show that wet etching a structure in a periphery of a semiconductor wafer is done by locally applying an etchant. Fishkin did not disclose a cathode, as the above rejection indicates. Rather, Potter was relied upon to teach that processes and equipment used to manufacture semiconductor wafers (i.e. the wafer of Fishkin locally wet etched in the periphery to uncover a structure) can be used during FED fabrication processes (i.e. the cathode of the FED as recited by AAPA and

Potter). One of ordinary skill in the art would be motivated to combine these references (i.e. the process of AAPA and Fishkin to the cathode of Potter) to obtain the benefits taught by Potter, i.e. allowing for a wide range of materials with less stringent controls of material purity.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter J Macchiarolo whose telephone number is (571) 272-2375. The examiner can normally be reached on 8:30 - 5:00, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on (571) 272-2475. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

pjm

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